FIG.1

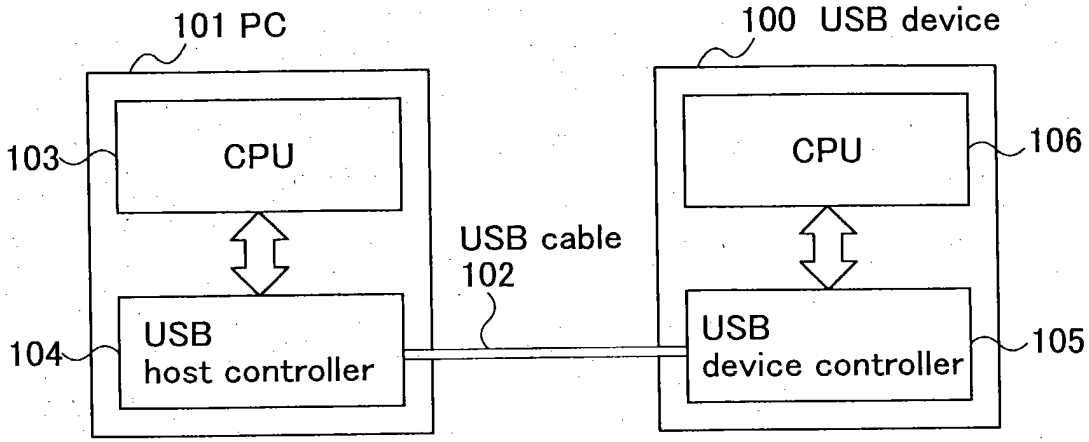

101 PC
100 USB device
CPU
CPU
103
106
USB cable
102
USB
host controller
USB
device controller
104
105

FIG.2

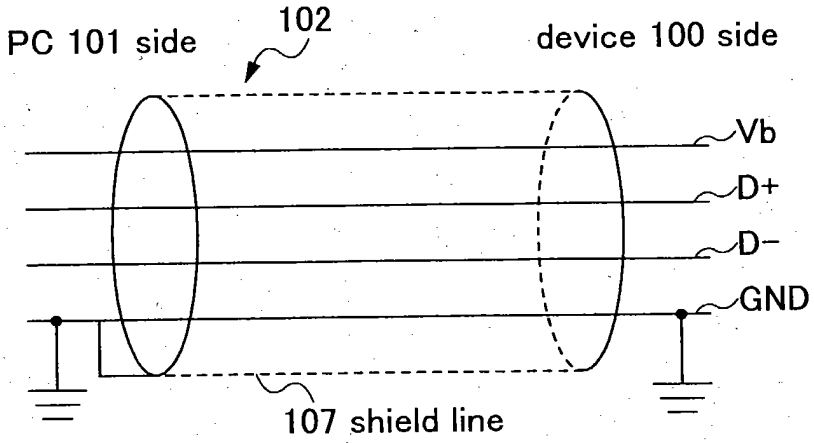

PC 101 side
102
device 100 side
Vb
D+
D−
GND
107 shield line

FIG.3

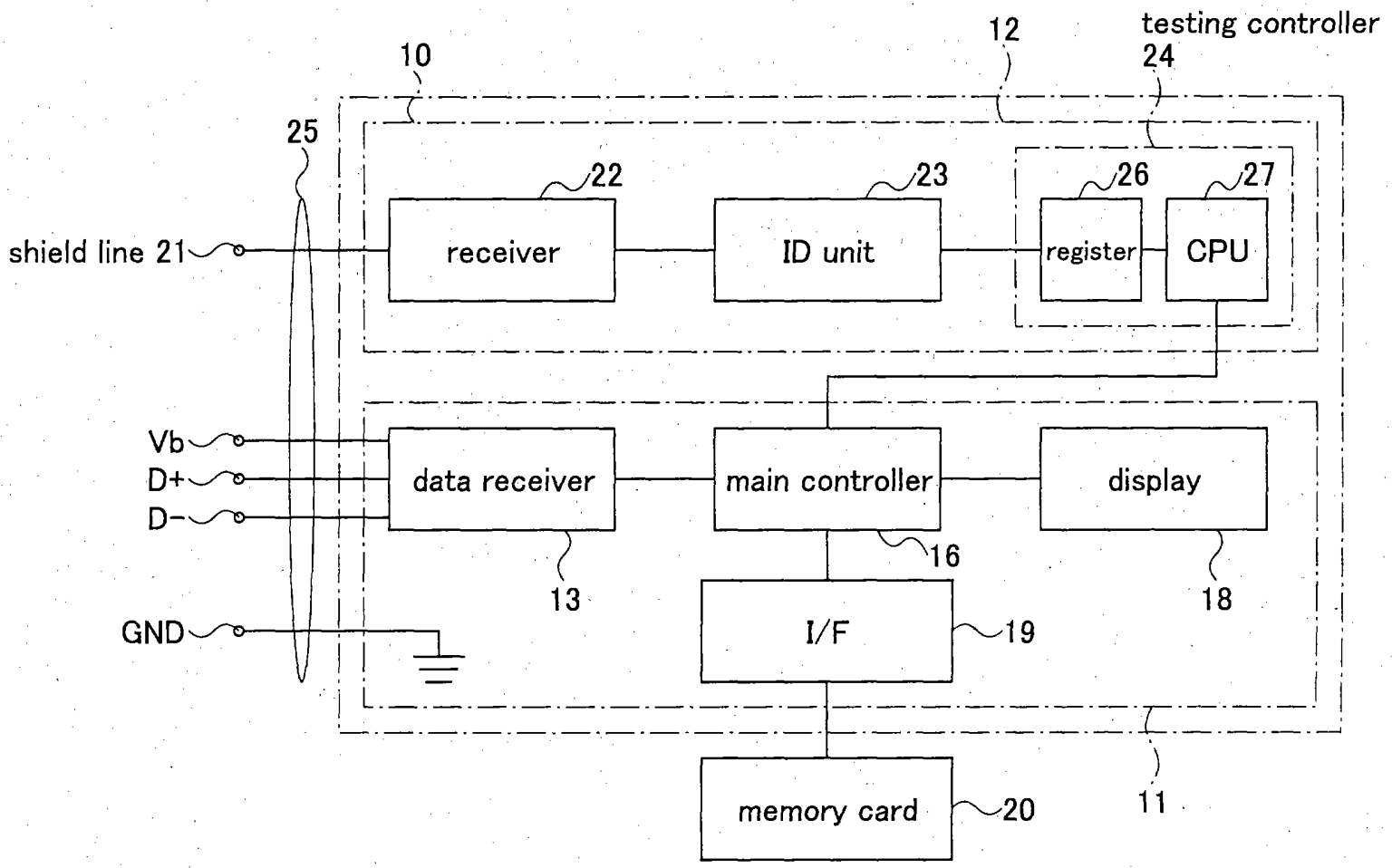

10
12
testing controller
24
25
22
23
26
27
shield line 21
receiver
ID unit
register
CPU
Vb
D+
D-
data receiver
main controller
display
16
13
18
GND
I/F
19
memory card
20
11

FIG.4

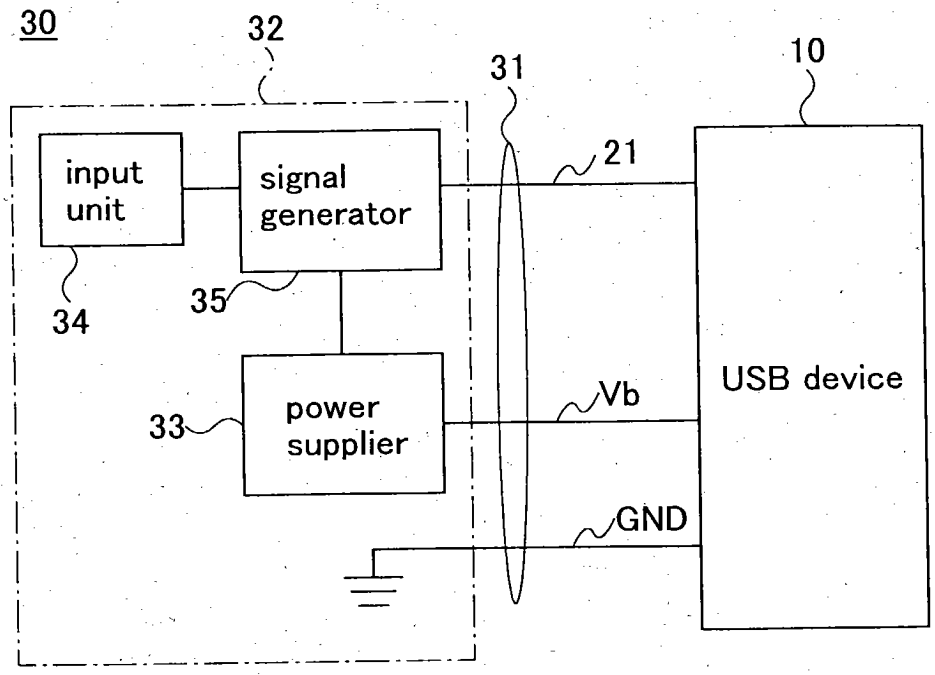

30
32
31
10
input unit
signal generator
21
34
35
power supplier
33
Vb
USB device
GND

FIG.5

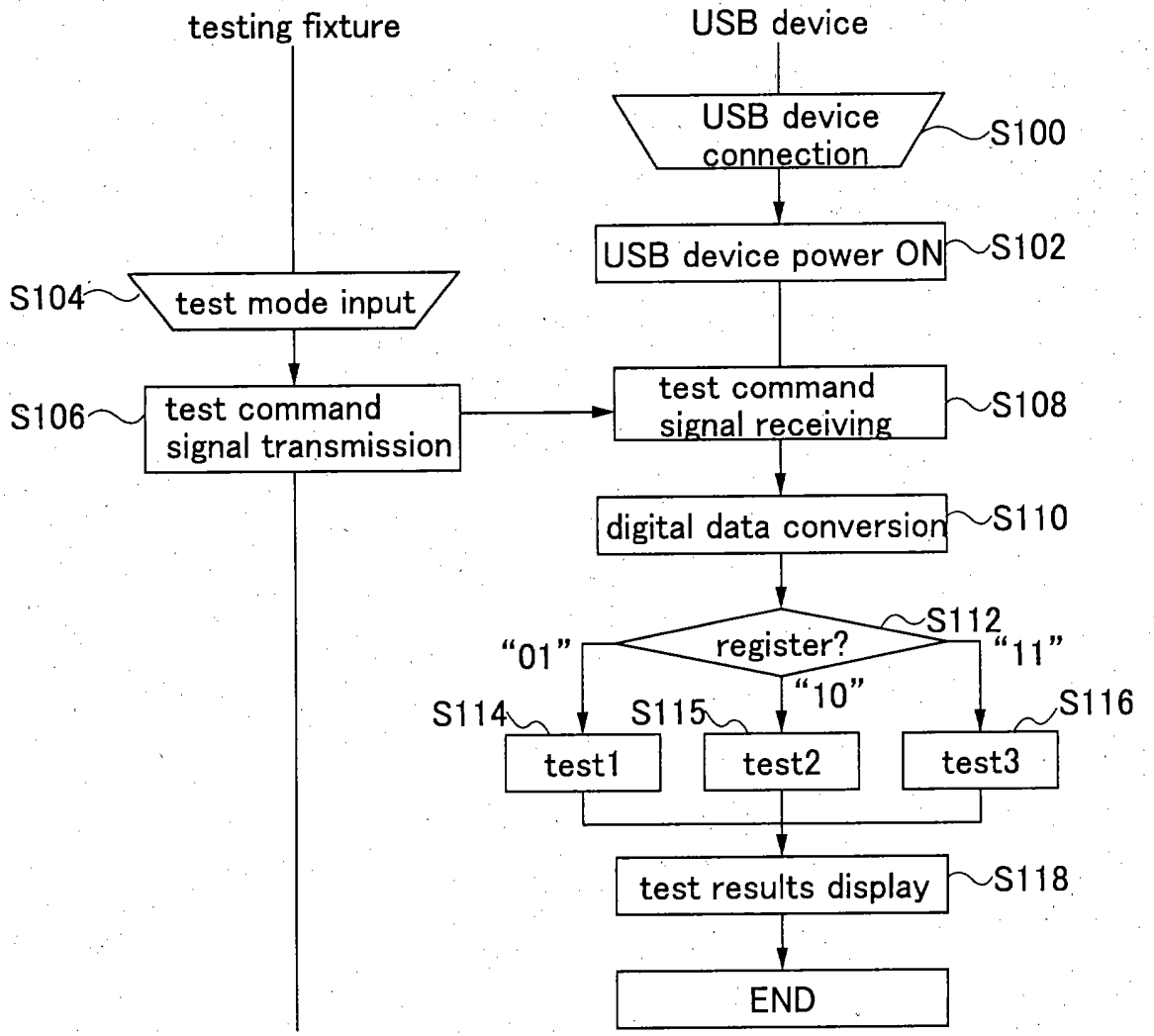

testing fixture
USB device
USB device connection
S100
USB device power ON
S102
S104
test mode input
S106
test command signal transmission
test command signal receiving
S108
digital data conversion
S110
S112
register?
"01"
"10"
"11"
S114
S115
S116
test1
test2
test3
test results display
S118
END

FIG.6

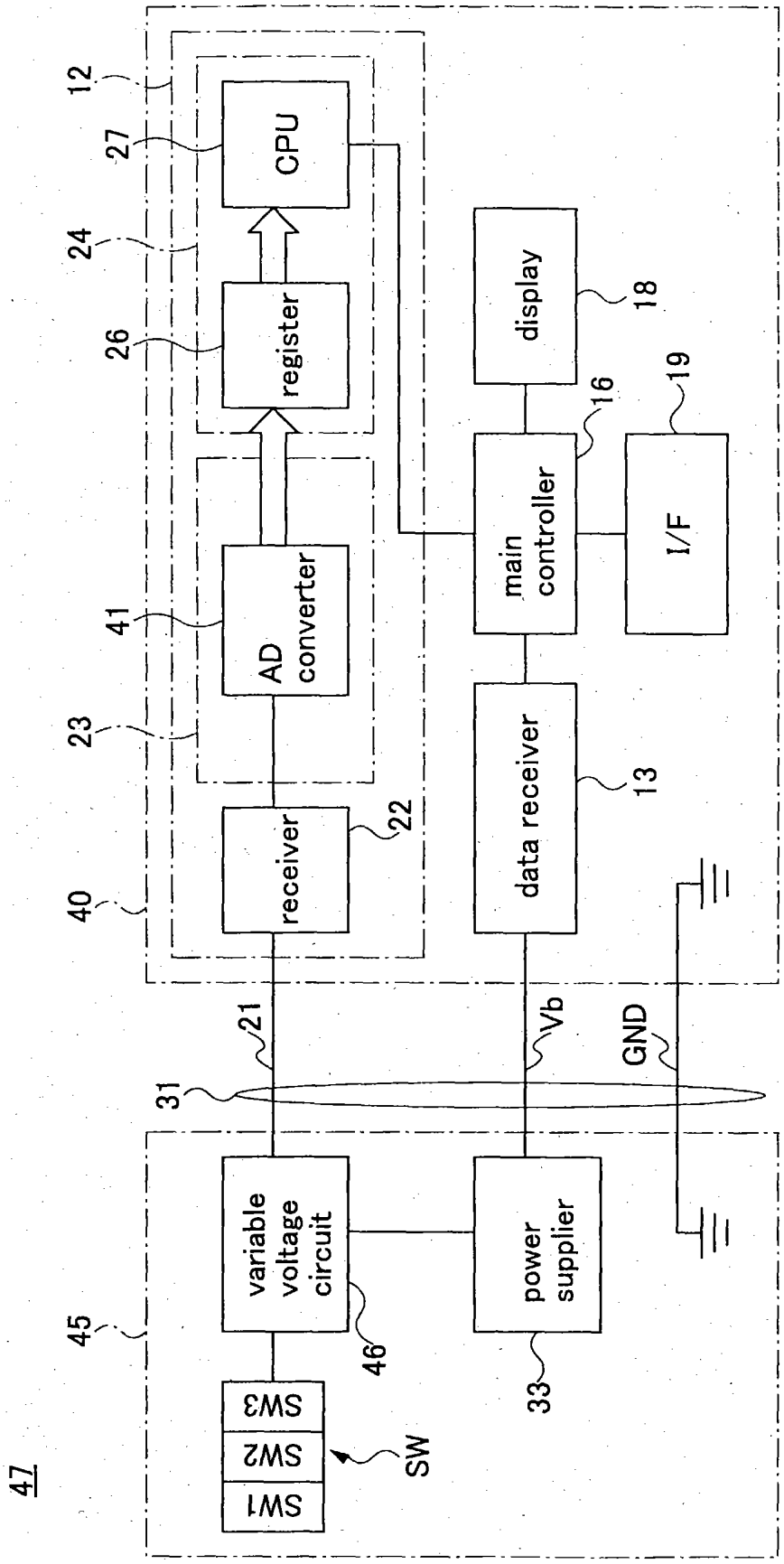

47
12
27
CPU
24
26
register
41
AD converter
23
40
receiver
22
display
18
16
main controller
19
I/F
data receiver
13
21
31
Vb
GND
45
variable voltage circuit
46
power supplier
33
SW3
SW2
SW1
SW

FIG.7

state of switch	testing command signal	state of register	test mode
SW1 SW2 SW3 ON OFF OFF	1V	MSB LSB 0 1	test1
OFF ON OFF	2V	1 0	test2
OFF OFF ON	3V	1 1	test3
OFF OFF OFF	0V	0 0	no test

FIG.8

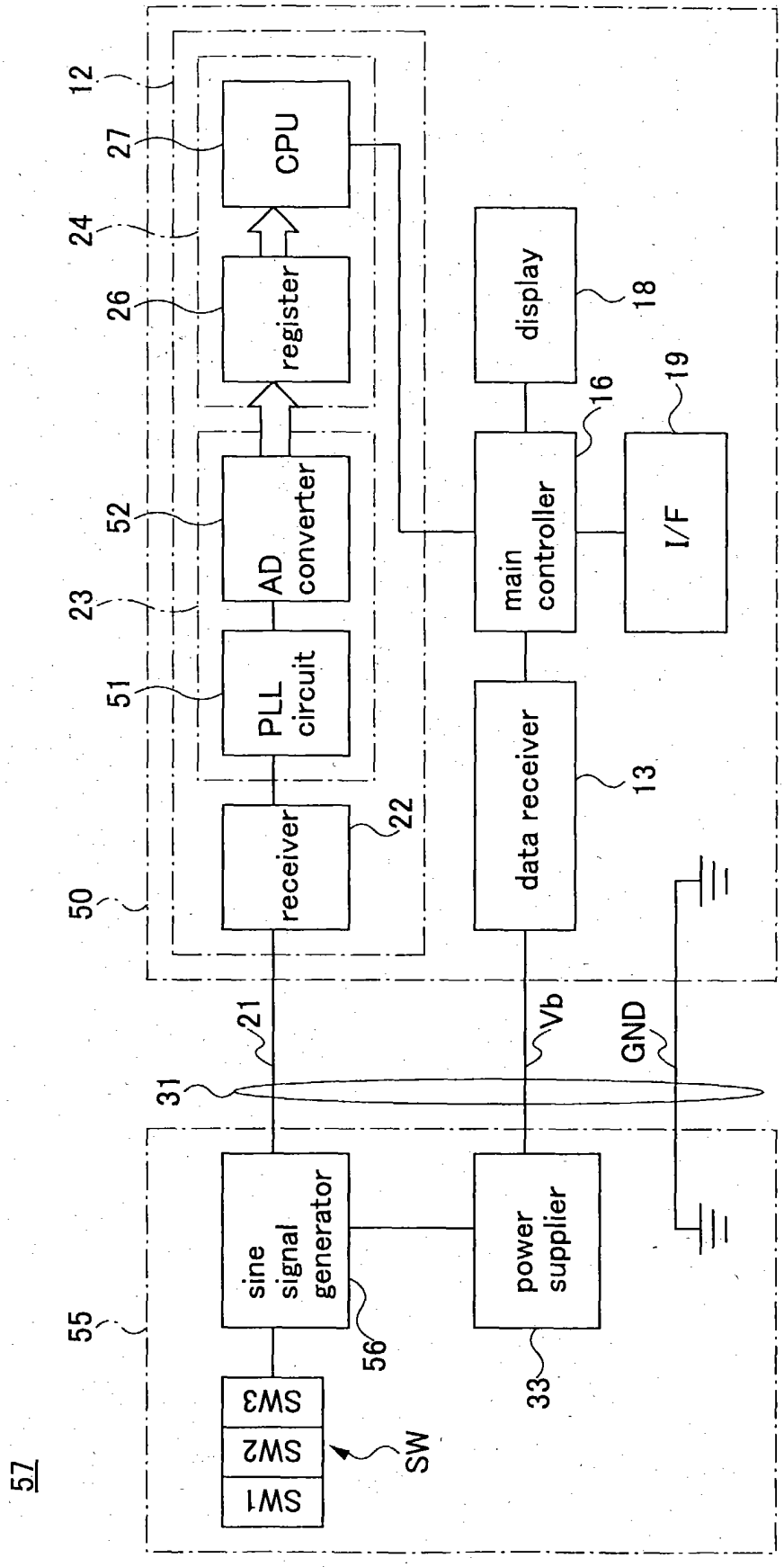

57
12
27
CPU
24
26
register
display
18
16
19
52
AD converter
main controller
I/F
23
51
PLL circuit
50
receiver
22
data receiver
13
21
Vb
GND
31
55
sine signal generator
power supplier
56
33
SW3
SW2
SW1
SW

FIG.9

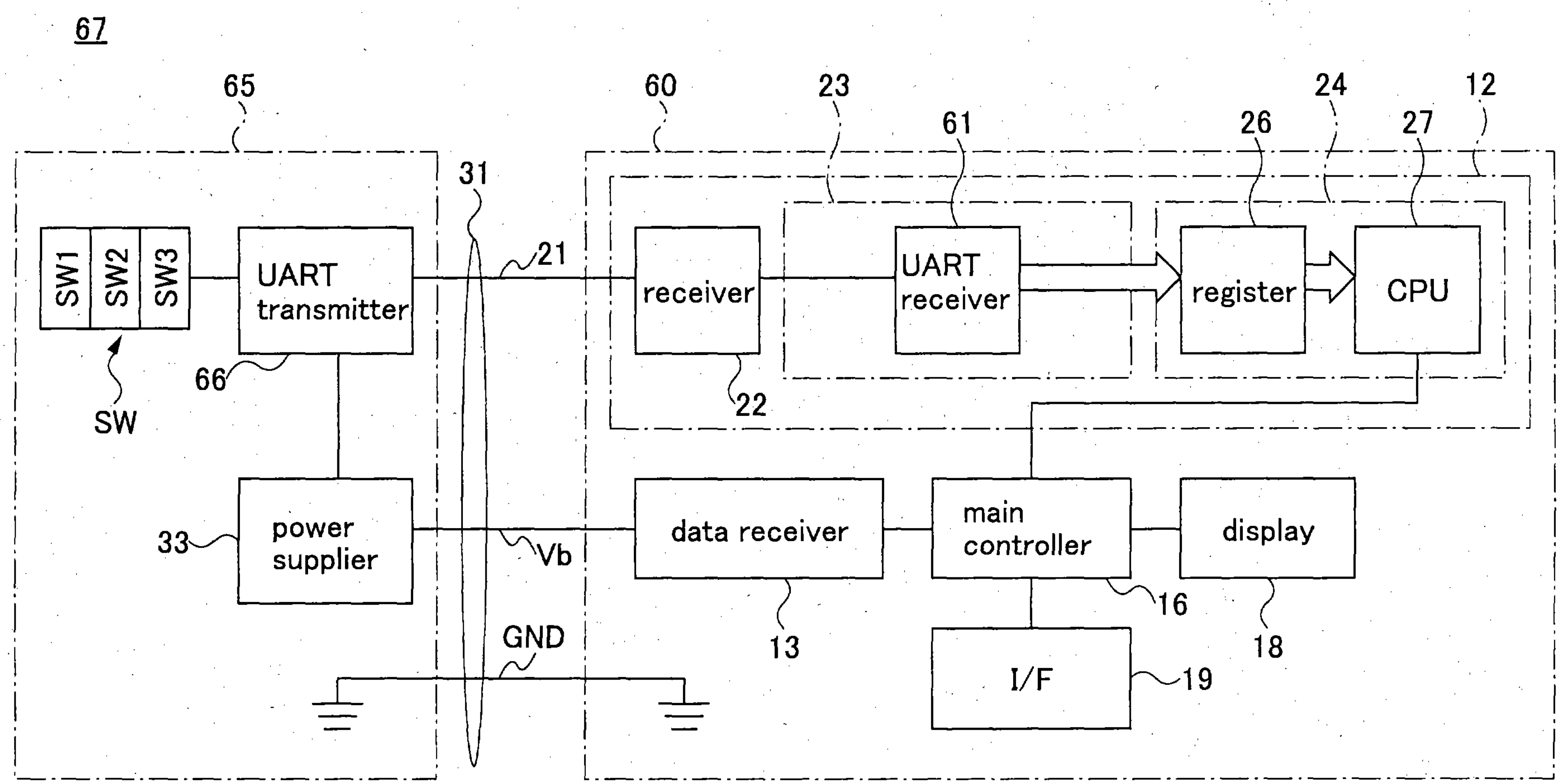

67
65
60
23
61
26
24
27
12
31
SW1
SW2
SW3
UART transmitter
21
receiver
UART receiver
register
CPU
66
SW
22
33
power supplier
Vb
data receiver
main controller
display
16
18
13
GND
I/F
19

FIG.10

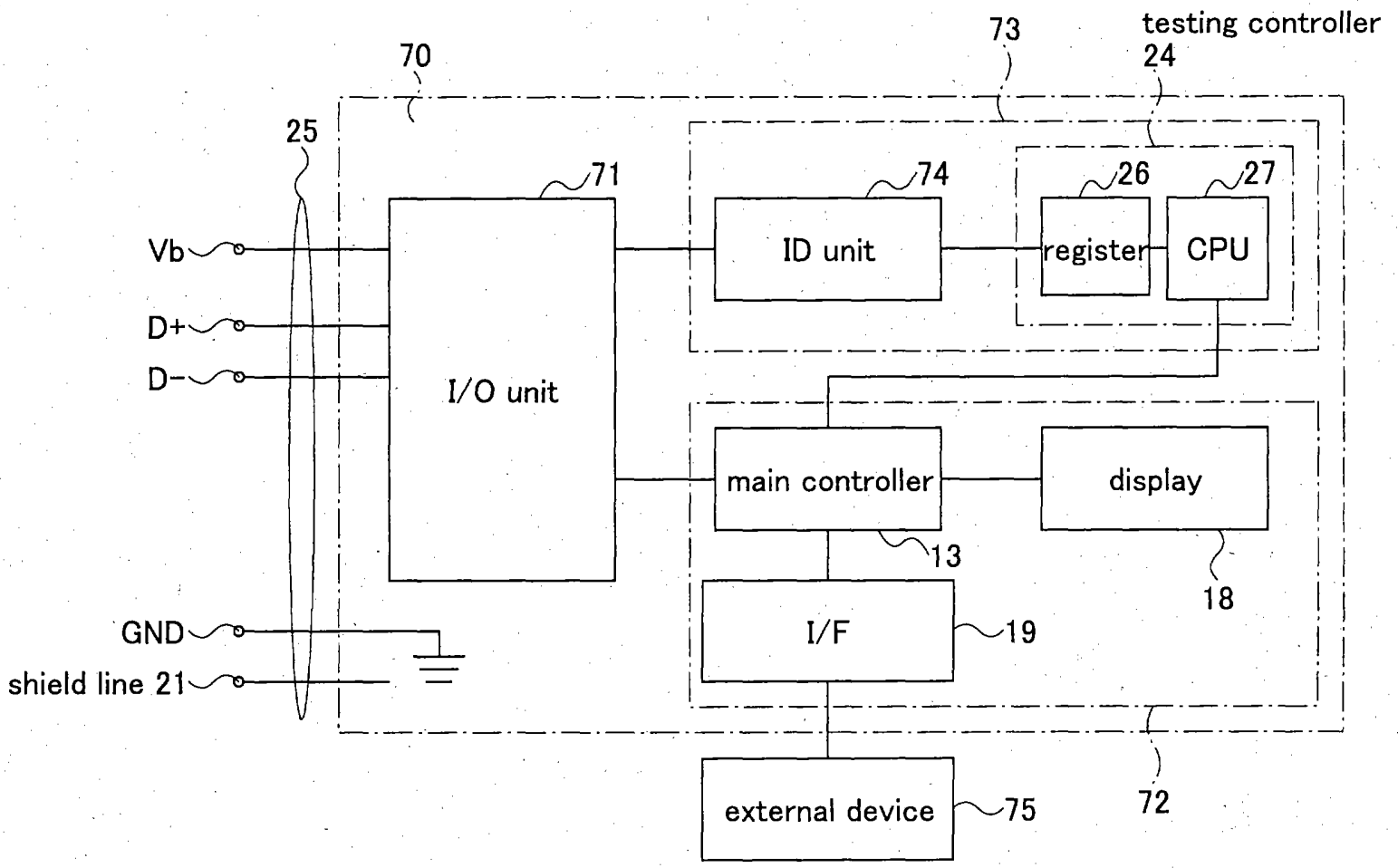

70
73
testing controller
24
25
71
74
26
27
Vb
D+
D−
I/O unit
ID unit
register
CPU
main controller
display
13
18
GND
shield line 21
I/F
19
external device
75
72

FIG.11

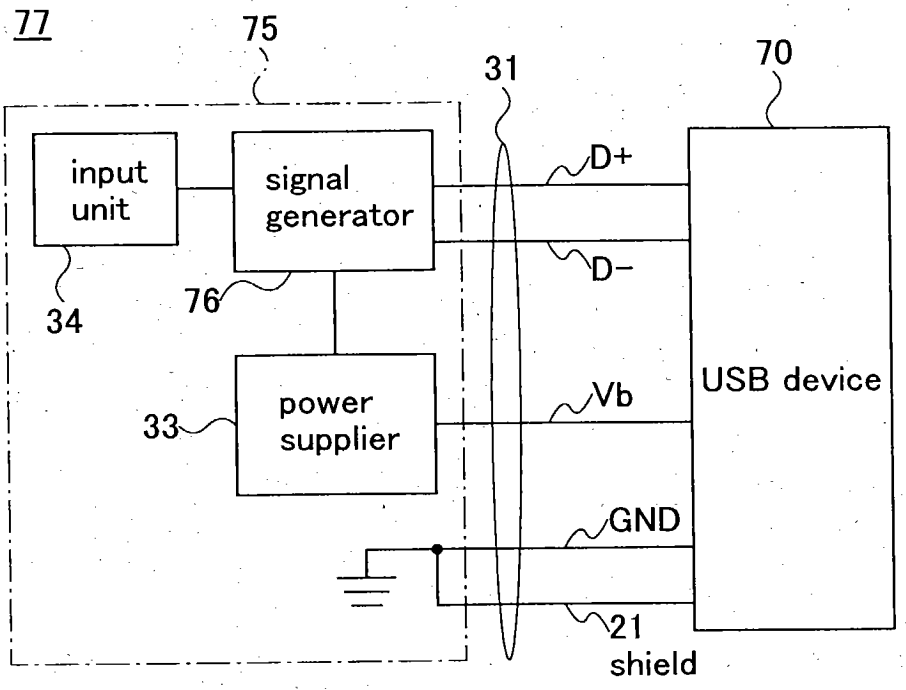

77
75
31
70
input unit
signal generator
D+
D−
34
76
power supplier
33
Vb
USB device
GND
21
shield

FIG.12

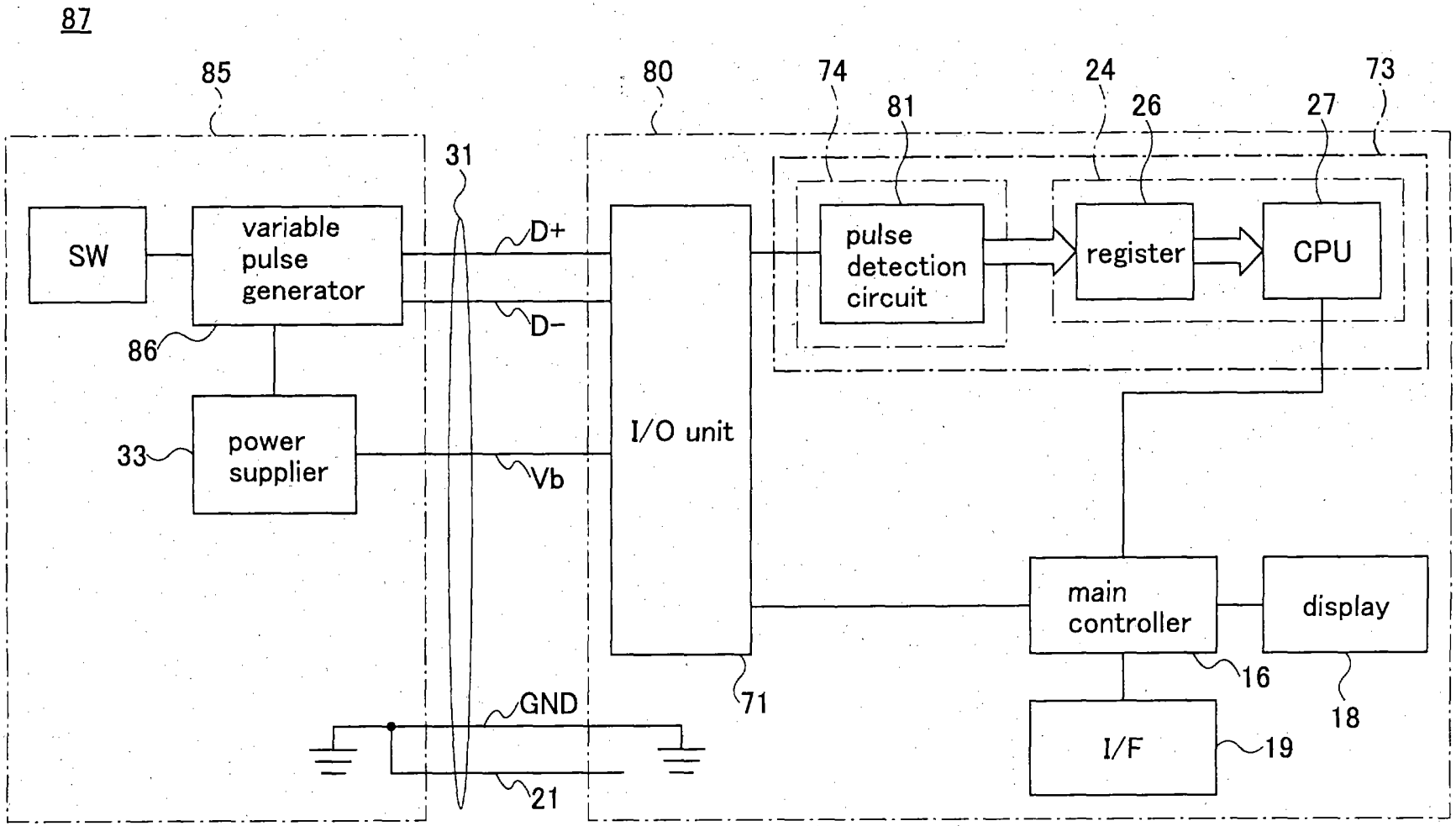
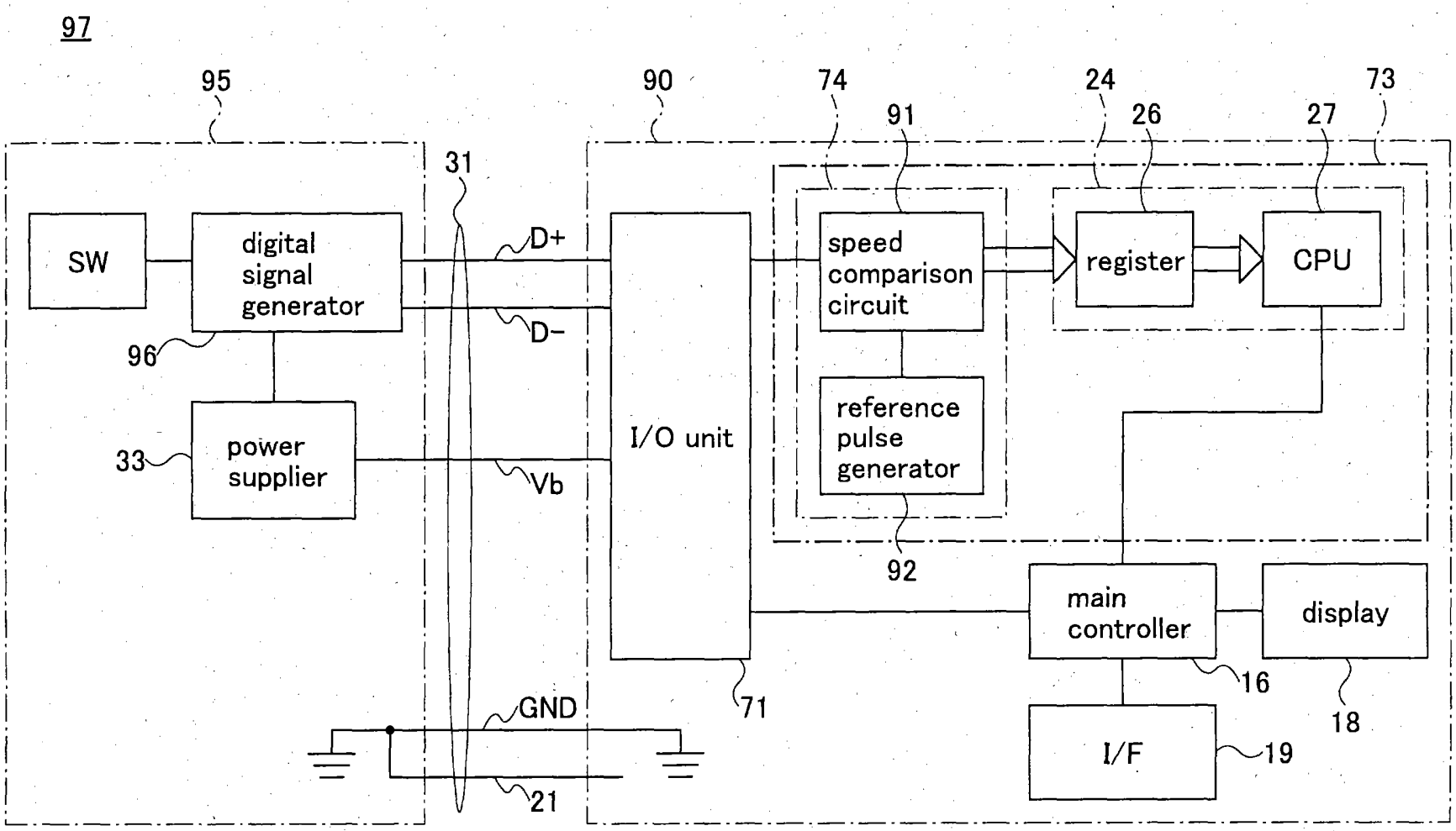

87
85
80
74
24
73
81
26
27
31
SW
variable pulse generator
D+
D-
86
33
power supplier
Vb
I/O unit
pulse detection circuit
register
CPU
main controller
display
16
18
71
GND
I/F
19
21

FIG.13


97
95
90
74
24
73
91
26
27
31
SW
digital signal generator
D+
D-
96
33
power supplier
Vb
I/O unit
speed comparison circuit
register
CPU
reference pulse generator
92
main controller
display
16
18
71
GND
21
I/F
19